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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TAKAOKA, DEAN O	

ART UNIT	PAPER NUMBER
2817	

NOTIFICATION DATE	DELIVERY MODE
12/12/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/586,748	HANGAI ET AL.	
	Examiner	Art Unit	
	DEAN O. TAKAOKA	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/21/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement filed July 21, 2006 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because corresponding title of each document has not been listed. It appears only the volume-issue has been listed. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Drawings

Figures 1 – 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Figure 1 is disclosed as conventional (page 5, line 5). Figures 2 and 3 are equivalent circuits of figure 1 thus also conventional.

Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective

action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

I) Claims 4 – 8, 10 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01.

The omitted elements are: In claim 4, a first field-effect transistor switch appears to be omitted. Claim 4 discloses a “second field-effect transistor switch” but a first field-effect transistor switch is not named thus the second field-effect transistor switch is actually the first FET or the first FET has been omitted or claim 4 should be dependent from claim 1. Accordingly, the claims are rejected under 35 U.S.C. 112 second paragraph as being incomplete for omitting essential elements, such omission amounting to a gap between the elements.

II) Claim 4 – 8, 10 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites the limitation/s “its ON state and OFF state” in page 33, line 5 and "its parasitic inductor" in page 33, line 8. There is insufficient antecedent basis for this limitation/s in the claim.

The limitation/s “its ON state and OFF state” and "its parasitic inductor" (suggests a previous recitation of an “ON state and OFF state” and “parasitic inductor” where none can be found in the claim thus there is insufficient antecedent basis for this limitation in the claim. Accordingly, the claims are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In the interest of advancing the prosecution and in so far as can be understood, the claims are examined below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 3 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakahara et al. (US 5,485,130).

1. Nakahara (Figs. 1, 7 et al.) shows an SPST (single-pole single-throw) switch for controlling propagation of a high frequency signal between an input terminal (15) and an output terminal (16), said SPST switch comprising: a plurality of first field-effect transistor switches connected in parallel (7a,b), each of which includes a field-effect transistor having its drain and source connected in parallel with an inductor (8a, b), wherein each of said field-effect transistors has its ON state and OFF state changed by

a voltage applied to a gate of each of said field-effect transistors (6a, b), and each of said field-effect transistors has its OFF capacitance cause parallel resonance with said inductor connected at a frequency of the high frequency signal (col. 1, lns 40-43).

2. The SPST switch according to claim 1, wherein said plurality of first field-effect transistor switches are connected in parallel between the input terminal (15) and output terminal (16).

3. The SPST switch according to claim 1, wherein the input terminal and the output terminal are connected to each other; and said plurality of first field-effect transistor switches are connected in parallel between the input terminal and a ground (shown).

9. An SPDT (single-pole double-throw) switch for controlling propagation of a high frequency signal between an input terminal and two output terminals, said SPDT switch employing: a plurality of first field-effect transistor switches as defined in claim 1, which are connected in parallel (where the signal is branched to output 2 or 3)..

Claims 1 – 3 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsunaga et al. (US 4,789,846).

1. Matsunaga (Fig. 6 et al.) shows an SPST (single-pole single-throw) switch for controlling propagation of a high frequency signal between an input terminal (node to 2) and an output terminal (nodes to 3 or 4), said SPST switch comprising: a plurality of first field-effect transistor switches connected in parallel (10, 14, 38), each of which includes a field-effect transistor having its drain and source connected in parallel with an inductor (5, 6, 43), wherein each of said field-effect transistors has its ON state and OFF state

changed by a voltage applied to a gate of each of said field-effect transistors (shown), and each of said field-effect transistors has its OFF capacitance cause parallel resonance with said inductor connected at a frequency of the high frequency signal (col. 8, lns 30-32).

2. The SPST switch according to claim 1, wherein said plurality of first field-effect transistor switches are connected in parallel between the input terminal (i.e. 2) and output terminal (i.e. 3 or 4).

3. The SPST switch according to claim 1, wherein the input terminal and the output terminal are connected to each other; and said plurality of first field-effect transistor switches are connected in parallel between the input terminal and a ground (shown).

9. An SPDT (single-pole double-throw) switch for controlling propagation of a high frequency signal between an input terminal and two output terminals, said SPDT switch employing: a plurality of first field-effect transistor switches as defined in claim 1, which are connected in parallel (where the signal is branched to 3 or 4).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumitsu et al. (JP 05-299995) prior art cited in Applicant's IDS of July 21, 2006 in view of Nakahara et al. (US 5,485,130) or Matsunaga et al. (US 4,789,846).

1. Tokumitsu (Fig. 6) shows an SPST (single-pole single-throw) switch for controlling propagation of a high frequency signal between an input terminal (25) and an output terminal (26 or 27), said SPST switch comprising: first field-effect transistor switch connected in parallel (4b), which includes a field-effect transistor having its drain and source connected in parallel with an inductor (L2), wherein said field-effect transistor has its ON state and OFF state changed by a voltage applied to a gate of each of said field-effect transistors (14'), and said field-effect transistors has its OFF capacitance cause parallel resonance with said inductor connected at a frequency of the high frequency signal (equation) but does not show a plurality of parallel connected field-effect transistors each having its drain and source connected in parallel with an inductor.

Nakahara or Matsunaga shows similar SPST switches comprising a plurality of field-effect transistor switches connected in parallel, which includes a plurality of field-effect transistor having its drain and source connected in parallel with an inductor (discussed in the reasons for rejection above).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the switch disclosed by Tokumitsu with the plural FET switches including parallel inductors disclosed by Nakahara et al. or Matsunaga et al. Such a modification would have been obvious where both circuits are drawn to

microwave switching; where each specific FET switch including parallel inductor and is resonant; where Nakahara teaches the advantage of maximum allowable value of incident power is increased in an antenna switch circuit (abstract); or where Matsunaga teaches solving the problems of increased manufacturing steps required for increased input power and allowing high voltages for decreased substrate area (col. 5, lns 23-37) thus suggesting the obviousness of the modification.

2. The SPST switch according to claim 1, wherein said plurality of first field-effect transistor switches are connected in parallel between the input terminal and output terminal (Nakahara – Figs. 1, 7 et al. or Matsunaga – Fig. 6).

3. The SPST switch according to claim 1, wherein the input terminal and the output terminal are connected to each other; and said plurality of first field-effect transistor switches are connected in parallel between the input terminal and a ground.

4. In so far as can be understood, an SPST (single-pole single-throw) switch for controlling propagation of a high frequency signal between an input terminal and an output terminal, said SPST switch comprising: a second field-effect transistor switch constructed by connecting an inductor in parallel with a series circuit of capacitor and a field-effect transistor that has its drain or source connected in series with the capacitor, wherein said field-effect transistor has its ON state and OFF state changed by a voltage applied to a gate of said field-effect transistor, and said field-effect transistor has its parasitic inductor and said capacitor cause series resonance, and has its OFF capacitance cause parallel resonance with said inductor (abstract – Tokumitsu).

5. The SPST switch according to claim 4, wherein said second field-effect transistor switch is connected between the input terminal and the output terminal.

6. The SPST switch according to claim 5, wherein a plurality of second field-effect transistor switches are connected in parallel between the input terminal and the output terminal (Matsunaga – Fig. 6).

7. The SPST switch according to claim 4, wherein the input terminal and the output terminal are connected to each other; and said second field-effect transistor switch is connected between the input terminal and a ground.

8. The SPST switch according to claim 7, wherein a plurality of second field-effect transistor switches are connected in parallel between the input terminal and the ground (see claim 6).

10. An SPDT (single-pole double-throw) switch for controlling propagation of a high frequency signal between an input terminal and two output terminals, said SPDT switch employing: a second field-effect transistor switch as defined in claim 4 (discussed in the reasons for rejection of Nakahara or Matsunaga above).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakahara et al. (US 5,485,130) or Matsunaga et al. (US 4,789,846) in view of Wallace et al. (US 6,137,377).

Nakahara or Matsunaga shows an SPST (single-pole single-throw) switch for controlling propagation of a high frequency signal between an input terminal and an

output terminal (discussed in the reasons for rejection of claim1 above) but does not show a MPMT (multiple-pole multiple throw) switch.

Wallace (Fig. 8) shows similar SPST switches comprising a plurality of field-effect transistor switches connected in parallel, which includes a plurality of field-effect transistor having its drain and source connected in parallel with an inductor further comprising a well-known MPMT (multiple-pole multiple throw) switch such as the double-pole multiple throw switch (cross coupled analogous to Applicant's Fig. 25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the switch disclosed by Nakahara or Matsunaga with the MPMT switch including parallel inductors disclosed by Wallace. Such a modification would have been obvious where both circuits are drawn to microwave switching; where each specific FET switch including parallel inductor and is resonant; where Wallace teaches the advantage of providing a switching phase shift circuit in as by example a microwave antenna system to enable single or dual polarity in the case of a planar antenna thus suggesting the obviousness of the modification.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumitsu et al. and Nakahara et al. or Matsunaga et al. as applied to claim 4 above, and further in view of Wallace et al. (US 6,137,377).

Tokumitsu and Nakahara or Matsunaga show a SPST (single-pole single-throw) switch for controlling propagation of a high frequency signal between an input terminal

and an output terminal (discussed in the reasons for rejection of claim4 above) but does not show a MPMT (multiple-pole multiple throw) switch.

Wallace (Fig. 8) shows similar SPST switches comprising a plurality of field-effect transistor switches connected in parallel, which includes a plurality of field-effect transistor having its drain and source connected in parallel with an inductor further comprising a well-known MPMT (multiple-pole multiple throw) switch such as the double-pole multiple throw switch (cross coupled analogous to Applicant's Fig. 25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the switch disclosed by Tokumitsu and Nakahara or Matsunaga with the MPMT switch including parallel inductors disclosed by Wallace. Such a modification would have been obvious where both circuits are drawn to microwave switching; where each specific FET switch including parallel inductor and is resonant; where Wallace teaches the advantage of providing a switching phase shift circuit in as by example a microwave antenna system to enable single or dual polarity in the case of a planar antenna thus suggesting the obviousness of the modification.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DEAN O. TAKAOKA whose telephone number is (571)272-1772. The examiner can normally be reached on 9:00a - 5:30p Mon - Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dean O Takaoka/
Primary Examiner, Art Unit 2817